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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/493,319	01/28/2000	Samson Huang	INTL-0312-US (P7995)	2102

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EXAMINER	
JORGENSEN, LELAND R	
ART UNIT	PAPER NUMBER
2675	5

DATE MAILED: 06/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/493,319	HUANG, SAMSON	
	Examiner	Art Unit	
	Leland R. Jorgensen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1 – 3, 5, 6, 8, 9, 11, 12, 15, 16, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakajima, USPN 6,333,737 B1.

Claim 1

Claim 1 describes a method comprising the following steps.

Capacitor. Claim 1 describes providing a capacitor to maintain a terminal voltage of a pixel cell near a predetermined voltage. Nakajima teaches providing a storage capacitor for each pixel. Nakajima, col. 1, lines 13 – 21; col. 2, line 67 – col. 3, line 5; col. 3, lines 22 – 25; and figure 1.

Memory. Claim 1 describes providing a memory to store a digital indication of the predetermined voltage. Nakajima teaches providing a memory 22 for each pixel. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1a.

Converting Digital to Analog. Claim 1 describes converting the digital indication into an analog voltage to update a charge on the capacitor. Nakajima teaches a digital to analog conversion circuit 25 at each pixel. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1. Nakajima does not specifically describe converting the digital indication into an analog voltage during a refresh operation, but it is inherent to the operation of such a circuit that the information would be changed during a refresh operation. See Nakajima, col. 1, lines 13 – 19.

Claim 2

RAM. Claim 2 is dependant on claim 1 and adds that the memory comprises a static random access memory RAM. Nakajima teaches that the memory may be a RAM. Nakajima, col. 3, lines 57 – 59.

Claim 3

Reading digital indication from memory. Claim 3 is dependant on claim 1 and adds the step of reading the digital indication from the memory during the refresh operation. Nakajima adds the step of reading the digital indication from the memory. Nakajima, col. 3, line 66 – col. 4, line 4; and col. 5, lines 51 – 52. Nakajima does not specifically describe the reading during the refresh operation, but it is inherent to the operation of such a circuit that the information would be changed during a refresh operation. See Nakajima, col. 1, lines 13 – 19.

Claim 5

Updating information with another digital indication. Claim 5 is dependant on claim 1 and adds the step of updating the memory with another digital indication of another predetermined voltage. Nakajima adds the step of updating the memory with another predetermined voltage. Nakajima, col. 3, lines 52 – 56; and col. 5, lines 42 – 50.

Claim 6

Claim 6 describes a method comprising the following steps.

Capacitor. Claim 6 describes providing capacitors, each capacitor being associated with a different pixel cell to maintain a terminal voltage of the associated pixel cell near a predetermined voltage. Nakajima teaches providing a storage capacitor for each pixel. Nakajima, col. 1, lines 13 – 21; col. 2, line 67 – col. 3, line 5; col. 3, lines 22 – 25; and figure 1.

Memory. Claim 6 describes providing memory buffers, each buffer being associated with a different one of the pixel cells and storing a digital indication of the associated predetermined voltage. Nakajima teaches providing a memory 22 for each pixel. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1a.

Converting Digital to Analog. Claim 6 describes converting the digital indication into an analog voltage to update a charges on the capacitors. Nakajima teaches a digital to analog conversion circuit 25 at each pixel. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1. Nakajima does not specifically describe converting the digital indication into an analog voltage during a refresh operation, but it is inherent to the operation of such a circuit that the information would be changed during a refresh operation. See Nakajima, col. 1, lines 13 – 19.

Claim 8

RAM. Claim 8 is dependant on claim 6 and adds that the memory buffers comprise a part of a static random access memory RAM. Nakajima teaches that the memory may be a RAM. Nakajima, col. 3, lines 57 – 59.

Claim 9

Reading digital indication from memory. Claim 9 is dependant on claim 6 and adds the step of reading the digital indication from the memory buffers during the refresh operation. Nakajima adds the step of reading the digital indication from the memory. Nakajima, col. 3, line 66 – col. 4, line 4; and col. 5, lines 51 – 52. Nakajima does not specifically describe the reading during the refresh operation, but it is inherent to the operation of such a circuit that the information would be changed during a refresh operation. See Nakajima, col. 1, lines 13 – 19.

Claim 11

Claim 11 (Amended) describes a light modulator cell comprising the following.

Pixel Cell. Claim 11 describes a pixel cell. Nakajima teaches a pixel 2 for a liquid crystal display. Nakajima, figures 1 and 2; col. 2, lines 44 – 47; and col. 3, lines 11 – 17.

Capacitor. Claim 11 describes a capacitor to maintain a terminal voltage of a pixel cell near a predetermined voltage. Nakajima teaches a storage capacitor at each pixel. Nakajima, col. 2, line 67 – col. 3, line 5; col. 3, lines 22 – 25; and figure 1.

Memory. Claim 11 describes a memory to store a digital indication of the predetermined voltage. Nakajima teaches a memory 22 at each pixel. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1.

Digital-to-Analog Converter. Claim 11 describes a digital-to-analog converter to convert the digital indication into an analog voltage to update a charge on the capacitor during a refresh operation. Nakajima teaches a digital to analog conversion circuit 25 at each pixel. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1. Nakajima does not specifically describe converting the digital indication into an analog voltage during a refresh operation, but it is inherent to the operation of such a circuit that the information would be changed during a refresh operation. See Nakajima, col. 1, lines 13 – 19.

Claim 12

RAM. Claim 12 is dependant on claim 11 and adds that the memory comprises a static random access memory RAM. Nakajima teaches that the memory may be RAM. Nakajima, col. 3, lines 57 – 59.

Claim 15

Updating information with another digital indication. Claim 15 is dependant on claim 11 and adds that the memory further is updated with another digital indication of another predetermined voltage. Nakajima teaches a circuit for updating the memory with another predetermined voltage. Nakajima, col. 3, lines 52 – 56; and col. 5, lines 42 – 50.

Claim 16

Claim 16 describes a light modulator cell comprising the following.

Pixel Cell. Claim 16 describes a pixel cell. Nakajima teaches a pixel 2 for a liquid crystal display. Nakajima, figures 1 and 2; col. 2, lines 44 – 47; and col. 3, lines 11 – 17.

Capacitor. Claim 16 describes capacitors, each capacitor being associated with a different pixel cell to maintain a terminal voltage of the associated pixel cell near a predetermined voltage. Nakajima teaches a storage capacitor associated with each pixel cell. Nakajima, col. 1, lines 13 – 21; col. 2, line 67 – col. 3, line 5; col. 3, lines 22 – 25; and figure 1.

Memory Buffer. Claim 16 describes memory buffers, each memory buffer being associated with a different one of the pixel cells and storing a digital indication of the associated predetermined voltage. Nakajima teaches a memory 22 associated with each pixel. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1.

Digital to Analog Converter. Claim 16 describes digital-to-analog converters to convert the digital indication into analog voltages to update charges on the capacitors during a refresh operation. Nakajima teaches a digital to analog conversion circuit 25 at each pixel. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1. Nakajima does not specifically describe converting the digital indication into an analog voltage during a refresh operation, but it is

inherent to the operation of such a circuit that the information would be changed during a refresh operation. See Nakajima, col. 1, lines 13 – 19.

Claim 18

RAM. Claim 18 is dependant on claim 16 and adds that at least one of the memory buffers comprises a part of a static random access memory. Nakajima teaches that the memory may be a RAM. Nakajima, col. 3, lines 57 – 59.

Claim Rejections - 35 USC § 103

3. Claims 4, 7, 10, 13, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima in view of Kinoshita et al, USPN 5,771,031.

Claim 4

Latching digital information. Claim 4 is dependant on claim 1 and adds the step of latching the digital indication from the memory during the refresh operation. As understood in the art, latching is holding data in a circuit until other circuits are ready to change the latch circuit.

Nakajima does not specifically teach the step of latching the information from the memory.

Kinoshita teaches the step of latching the information from the memory while the data is updated. Kinoshita, col. 6, lines 39 – 42; col. 6, lines 63 – col. 7, line 6; col. 7, lines 14 – 21, lines 46 – 67; and col. 9, line 59 – col. 10, line 67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method and circuits of Nakajima with the latching method and circuit of

Kinoshita. Like Nakajima, Kinoshita teaches a drive method for individual pixels of a flat panel display. Kinoshita, col. 1, lines 5 –8; and col. 3, lines 60 –65. Both Nakajima and Kinoshita teach many of the same parts including storage capacitors, CS, memory, and digital to analog converters. See e.g. Kinoshita, figures 1, 3 & 4; col. 4, lines 33 –36; col. 5, lines 64 – 66; col. 7, lines 14 – 21; and col. 8, lines 11 – 14. Both teach the need to individually drive each pixel array. Kinoshita, col. 1, line 10 – col. 2, line 37; and col. 2, lines 6 – 9. Kinoshita teaches that the memory can be reduced with its latching circuit. Kinoshita, col. 9, lines 59 – 67; and col. 10, lines 60 – 67.

Claim 7

Row of Pixels. Claim 7 is dependant on claim 6 and adds that the capacitors are associated with a row of pixels.

Nakajima does not specifically teach that the capacitors are associated with a row of pixels.

Kinoshita teaches that the capacitors are associated with a row of pixels. Kinoshita, col. 4, lines 19 – 22, lines 35 – col. 36, and lines 62 - 65.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method and circuits of Nakajima with the method and circuits of Kinoshita. Like Nakajima, Kinoshita teaches a drive method for individual pixels of a flat panel display. Kinoshita, col. 1, lines 5 –8; and col. 3, lines 60 –65. Both Nakajima and Kinoshita teach many of the same parts including storage capacitors, CS, memory, and digital to analog converters. See e.g. Kinoshita, figures 1, 3 & 4; col. 4, lines 33 –36; col. 5, lines 64 – 66; col. 7, lines 14 –

21; and col. 8, lines 11 – 14. Both teach the need to individually drive each pixel array. Kinoshita, col. 1, line 10 – col. 2, line 37; and col. 2, lines 6 – 9.

Claim 10

Latching digital information. Claim 10 is dependant on claim 6 and adds the step of latching the digital indication during the refresh operation.

Nakajima does not specifically teach the step of latching the information from the memory.

Kinoshita teaches the step of latching the information from the memory while the data is updated. Kinoshita, col. 6, lines 39 – 42; col. 6, lines 63 – col. 7, line 6; col. 7, lines 14 – 21, lines 46 – 67; and col. 9, line 59 – col. 10, line 67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method and circuits of Nakajima with the latching method and circuit of Kinoshita. Like Nakajima, Kinoshita teaches a drive method for individual pixels of a flat panel display. Kinoshita, col. 1, lines 5 –8; and col. 3, lines 60 –65. Both Nakajima and Kinoshita teach many of the same parts including storage capacitors, CS, memory, and digital to analog converters. See e.g. Kinoshita, figures 1, 3 & 4; col. 4, lines 33 –36; col. 5, lines 64 – 66; col. 7, lines 14 – 21; and col. 8, lines 11 – 14. Both teach the need to individually drive each pixel array. Kinoshita, col. 1, line 10 – col. 2, line 37; and col. 2, lines 6 – 9. Kinoshita teaches that the memory can be reduced with its latching circuit. Kinoshita, col. 9, lines 59 – 67; and col. 10, lines 60 – 67.

Claim 13

Claim 13 is dependant on claim 11 and adds the following.

Bit Latches and Sense Amplifiers. Claim 11 teaches bit latches and sense amplifiers to communicate the digital indication from the memory to the bit latches during the refresh operation. Nakajima teaches an operating unit 23a to communicate information from the memory to register circuit 24. Nakajima, col. 5, lines 51 – 66; and figure 1.

Nakajima does not specifically describe the register circuit as a bit latch.

Kinoshita teaches the step of latching the information from the memory while the data is updated. Kinoshita, col. 6, lines 39 – 42; col. 6, lines 63 – col. 7, line 6; col. 7, lines 14 – 21, lines 46 – 67; and col. 9, line 59 – col. 10, line 67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method and circuits of Nakajima with the latching method and circuit of Kinoshita. Like Nakajima, Kinoshita teaches a drive method for individual pixels of a flat panel display. Kinoshita, col. 1, lines 5 –8; and col. 3, lines 60 –65. Both Nakajima and Kinoshita teach many of the same parts including storage capacitors, CS, memory, and digital to analog converters. See e.g. Kinoshita, figures 1, 3 & 4; col. 4, lines 33 –36; col. 5, lines 64 – 66; col. 7, lines 14 – 21; and col. 8, lines 11 – 14. Both teach the need to individually drive each pixel array. Kinoshita, col. 1, line 10 – col. 2, line 37; and col. 2, lines 6 – 9. Kinoshita teaches that the memory can be reduced with its latching circuit. Kinoshita, col. 9, lines 59 – 67; and col. 10, lines 60 – 67.

Claim 14

Latching digital information. Claim 14 (Amended) is dependant on claim 11 and adds bit latches to latch the digital indication during the refresh operation.

Nakajima does not specifically teach latches to latch the information from the memory.

Kinoshita teaches latches to latch information from the memory while the data is updated. Kinoshita, col. 6, lines 39 – 42; col. 6, lines 63 – col. 7, line 6; col. 7, lines 14 – 21, lines 46 – 67; and col. 9, line 59 – col. 10, line 67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the circuits of Nakajima with the latching circuit of Kinoshita. Like Nakajima, Kinoshita teaches a drive method for individual pixels of a flat panel display. Kinoshita, col. 1, lines 5 –8; and col. 3, lines 60 –65. Both Nakajima and Kinoshita teach many of the same parts including storage capacitors, CS, memory, and digital to analog converters. See e.g. Kinoshita, figures 1, 3 & 4; col. 4, lines 33 –36; col. 5, lines 64 – 66; col. 7, lines 14 – 21; and col. 8, lines 11 – 14. Both teach the need to individually drive each pixel array. Kinoshita, col. 1, line 10 – col. 2, line 37; and col. 2, lines 6 – 9. Kinoshita teaches that the memory can be reduced with its latching circuit. Kinoshita, col. 9, lines 59 – 67; and col. 10, lines 60 – 67.

Claim 17

Row of Pixels. Claim 17 is dependant on claim 16 and adds that the capacitors are associated with a row of pixels.

Nakajima does not specifically teach that the capacitors are associated with a row of pixels.

Kinoshita teaches that the capacitors are associated with a row of pixels. Kinoshita, col. 4, lines 19 – 22, lines 35 – col. 36, and lines 62 - 65.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method and circuits of Nakajima with the method and circuits of Kinoshita. Like Nakajima, Kinoshita teaches a drive method for individual pixels of a flat panel display.

Kinoshita, col. 1, lines 5 –8; and col. 3, lines 60 –65. Both Nakajima and Kinoshita teach many of the same parts including storage capacitors, CS, memory, and digital to analog converters. See e.g. Kinoshita, figures 1, 3 & 4; col. 4, lines 33 –36; col. 5, lines 64 – 66; col. 7, lines 14 – 21; and col. 8, lines 11 – 14. Both teach the need to individually drive each pixel array. Kinoshita, col. 1, line 10 – col. 2, line 37; and col. 2, lines 6 – 9.

Response to Amendments

Drawings and Specification

4. The amendments have been noted and recorded. In view of the amendments to the abstract and drawing, the objections to the abstract and drawings are withdrawn.

Claim Rejections - 35 USC § 112

5. In view of the amendment to claim 14, the rejection under 35 U.S.C. 112 is withdrawn.

Response to Applicant's Traverse

Rejections of Claims 1 – 5

6. Applicant contents,

> Nakajiima neither teaches nor suggests that the DAC circuit 25 converts the digital indication from the output register circuit 24 into an analog voltage to update a charge on a capacitor during a refresh operation. Furthermore, Nakajiima does not mention a refresh operation in connection with its disclosed circuitry.
>
> Remarks, p. 3.

Nakajima, however, teaches, "The DAC circuit 25 has a function of converting digital data from the output register circuit 24 to analog data and outputting the analog data to a pixel

electrode as described later." Nakajima, col. 4, lines 24 – 27. See also Nakajima, col. 6, lines 22 –24. "The driving elements and the storage capacitors are provided at every pixel...." Nakajima, col. 2, line 67 – col. 3, line 2. Nakajima notes,

> In order to provide each pixel 2 with an operating function, not only the driving element and the storage capacitor, but also an input register circuit 21, a memory 22, an operation circuit 23, an output register circuit 24 and a digital-to-analog conversion circuit (hereinafter referred to as "DAC circuit") 25 are integrated on the element-formed layer 8 of each pixel as shown in FIG. 1, for example. ... In FIGS. 1 to 3, the driving elements, the storage capacitors, the source electrode lines and the gate electrode lines are omitted from the illustration.
>
> Nakajima, col. 3, lines 11 – 25.

Although Nakajima does not specifically use the term "refresh," it is inherent that the conversion takes place during a refresh operation. To refresh an image means "To redraw an image on a non-permanent display surface." The New IEEE Standard Dictionary of Electrical and Electronics Terms, 5th Ed., 1993, p. 1101. Thus, anytime a voltage is applied to an integrated pixel of a display, the image is redrawn on the pixel and a refresh operation takes place.

Therefore, Examiner's rejections of claims 1 – 5 remain unchanged.

Rejections of Claims 6 – 10, 11 – 15, and 16 - 18

7. For the reason stated above, Examiner's rejections of Claims 6 – 10, 11 – 15, and 16 – 18 also remain unchanged.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland Jorgensen whose telephone number is 703-305-2650. The examiner can normally be reached on Monday through Friday, 7:00 a.m. through 3:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven J. Saras can be reached on 703-305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, telephone number (703) 306-0377.

lrj

STEVEN SARAS
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